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06ES33

Third Semester B.E. Degree Examination, December 2011
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***1. Answer any FIVE full questions, selecting at least TWO questions from each part.***
2. Standard notations are used.
3. Missing data be suitably assumed.
4. Draw, diagrams wherever necessary.

PART – A

1 a. Write the steps for converting a verbal problem statement into truth table. **(05 Marks)**

b. A conveyor system brings raw material in from three different sources. The three sources converge into a single output conveyor. Sensors mounted adjacent to each source conveyor indicates the presence of raw material. All four conveyors have separate motors so they can be individually controlled (on/off). It is required to design a on/off control system of motors to meet the following conditions :
If sources has the product, then sources 2 and 3 must be turned off ; if source 1 is empty, then either source 2 or 3 or both can be turned on. In the event that no product is available form the three sources, the output conveyor must be turned off. If no product is available, the respective source conveyor must be turned off i) Determine the number of inputs and outputs ; ii) Construct the truth table that describes the system. **(05 Marks)**

c. Simplify the following Boolean function and realize the simplified expression using NAND gates : $F(v, w, x, y, z) = \sum m (3, 7, 8, 10, 11, 12, 14, 15, 17, 19, 21, 23, 25, 27, 29, 31) + \sum d (2, 6, 16, 20)$. **(10 Marks)**

2 a. For the Boolean function $f(w, x, y, z) = \sum m (0, 1, 3, 7, 8, 12) + \sum d (5, 10, 13, 14)$
i) Find the set of prime implicants and ii) Obtain the minimal SOP expressions using QM method. **(12 Marks)**

b. Simplify the Boolean function $f(w, x, y, z) = \sum m 1, 2, 3, 6, 7, 10, 14, 15)$ using MEV K – map with variable z as MEV. **(08 Marks)**

3 a. Write the truth table of IC 74LS147 and draw the set up to interface keypad of decimal digits to the digital system using IC 74LS147. Briefly explain the operation of interface set up. (IC 74LS147 : Decimal – to – BCD priority encoder). **(10 Marks)**

b. Design a combinational circuit using two 74LS138 ICs and NAND gates that generates a logic 1 output when a majority of four inputs are true (logic 1). (IC 74LS138 : 3 – to – 8 decoder). **(10 Marks)**

4 a. Construct the truth table of a full subtractor and realize using IC 74LS153. (IC74LS153 : Dual 4:1 multiplexer). **(06 Marks)**

b. Design a single – digit BCD adder using ICs 7483 having binary – to – BCD conversion logic (IC7483 : 4 – bit parallel adder). **(10 Marks)**

c. Sketch a diagram using two 74LS85ICs to compare (IC74LS85 : 4 – bit magnitude comparator). **(04 Marks)**

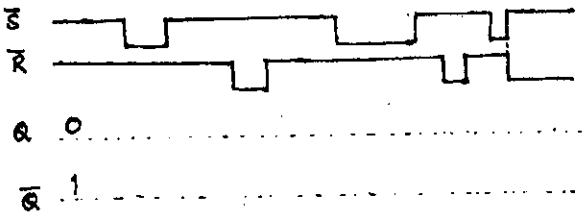
PART – B

5 a. Explain, how to use SR latch as a switch debouncer. Draw the timing diagram to support your explanation. **(07 Marks)**

b. Draw the logic diagram of master – salve JK flip – flop using gates. Write its function table and derive the characteristic equation. What is the type of triggering used in master – slave flip – flops? **(09 Marks)**

c. In the figure shown in Fig.Q.5(c), complete the timing diagram for a NAND latch. **(04 Marks)**

Fig.Q.5(c)

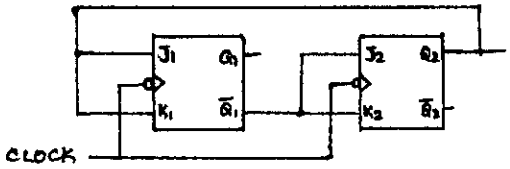


6 a. Draw the logic diagram of a 4-bit universal shift register using 4:1 multiplexers. Write its mode control table. **(06 Marks)**

b. Design a synchronous mod – 6 counter whose counting sequence is 0, 1, 2, 4, 6, 7 and repeat, by obtaining its minimal – sum equations. Use positive – edge – triggered D flip – flops. **(10 Marks)**

c. In the figure shown in Fig.Q.6(c) sketch the counting sequence. Assume both the flip – flops are cleared initially. **(04 Marks)**

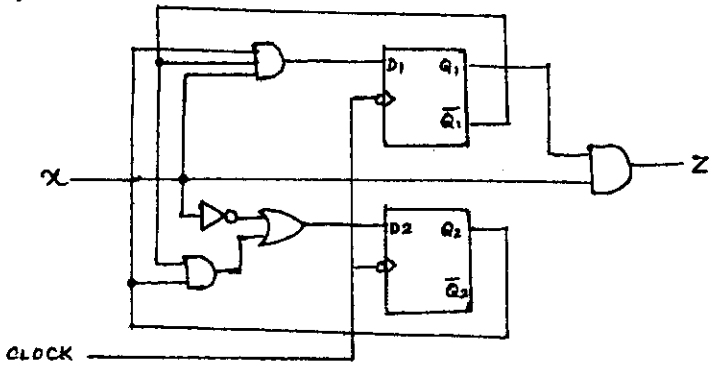
Fig.Q.6(c)



7 a. Describe the following terms with respect to sequential machines :
i) State ; ii) Present state ; iii) Next state. **(06 Marks)**

b. For the logic diagram shown in Fig.Q.7(b) :
i) Write the excitation and output functions.
ii) Form the excitation table, transition table, and state table
iii) Draw the state diagram and
iv) Is this a mealy machines or Moore machine? **(14 Marks)**

Fig.Q.7(b)



8 a. Construct a state diagram that will detect a serial input sequence of 0101. The required bit pattern can occur in a long data string and the correct pattern can overlap with another pattern. When the input pattern has been detected, cause the output z to be asserted high. Design the sequential machine using D flip – flops. Use the state assignments, A → 00, B → 01, C → 10 , D → 11. **(14 Marks)**

b. Draw the logic diagram of mod-8 twisted - ring counter. Write its counting sequence. **(06 Marks)**

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